IN THE CLAIMS

Re-write Claims 7, 13 and 21 as follows. Cancel Claims 1-6 and 18. Add new Claim 22 as follows.

1-6 (Canceled)

7. (Currently Amended) A method of fabricating a fieldless array, the method comprising:

forming an oxide-nitride-oxide (ONO) layer over a surface of a semiconductor region;

patterning the ONO layer to create a first set of ONO structures that define locations for a plurality of diffusion bit lines of the fieldless array; then

forming a plurality of word lines over the first set of ONO structures; and then

patterning the first set of ONO structures, thereby creating a second set of ONO structures, wherein the second set of ONO structures are located entirely under the plurality of word lines.

8. (Original) The method of Claim 7, further comprising forming dielectric sidewall spacers adjacent to the word lines.

9. (Original) The method of Claim 7, further comprising forming gap-filling oxide between the word lines.

10. (Original) The method of Claim 7, further comprising implanting diffusion bit lines through the first set of ONO structures.

11. (Original) The method of Claim 10, further comprising thermally growing bit line oxide regions over the diffusion bit lines.

12. (Original) The method of Claim 10, wherein the diffusion bit lines extend along a first axis, and the word lines extend along a second axis, perpendicular to the first axis.

13. (Currently Amended) The method of Claim 7 ~~10~~, wherein the steps of forming a plurality of word lines and patterning the first set of ONO structures comprise:

depositing a layer of polysilicon over the first set of ONO structures;

forming a photoresist mask over the layer of polysilicon;

etching the layer of polysilicon through the photoresist mask; and

etching the first set of ONO structures through the photoresist mask

14. (Original) The method of Claim 13, wherein the steps of etching the layer of polysilicon and the first set of ONO structures are implemented by a reactive ion etch (RIE).

15. (Original) The method of Claim 13, wherein the step of etching the first set of ONO structures is implemented by a series of wet etches.

16. (Original) The method of Claim 13, wherein the step of etching the first set of ONO structures is implemented by a wet etch and a dry/reactive ion etch (RIE).

17. (Original) The method of Claim 13, wherein the step of etching the first set of ONO structures is extended to etch the semiconductor substrate to a depth of 50 to 400 Angstroms.

18. (Canceled)

19. (Original) The method of Claim 13, further comprising performing a re-oxidation step after the step of etching the first set of ONO structures.

20. (Original) The method of Claim 19, wherein the re-oxidation step results in the formation of about 20-200 Angstroms of silicon oxide.

21. (Currently Amended) The method of Claim 13, wherein the step of etching the first set of ONO structures results in the removal of portions of the first set of ONO structures under the layer of polysilicon.

22. (New) The method of Claim 7, wherein the steps of forming a plurality of word lines and patterning the first set of ONO structures comprise:

depositing a layer of polysilicon over the first set of ONO structures;

patterning the layer of polysilicon;

depositing a thin dielectric spacer having a thickness up to about 400 Angstroms over the patterned layer of polysilicon;

etching back the thin dielectric spacer layer, prior to etching the first set of ONO structures.

etching the first set of ONO structures through the etched back thin dielectric spacer layer.